REMARKS

I. Introduction

These amendments and remarks are being filed in response to the Office Action dated April 23, 2008. Claims 1-13, 15, 18 and 19 are pending. Claims 14, 16 and 17 were previously cancelled. Claims 5, 6, 9-11 18 and 19 were withdrawn by the Examiner following a Restriction Requirement.

Applicants acknowledge, with appreciation, the Examiner's objection to Claim 4 as being dependent on a rejected base claim but being allowable if re-written in independent form. As such, claim 4 has been re-written in independent form, including all of the elements of independent claim 1 and intervening claim 3.

Claim 13 has been amended to maintain proper antecedent basis.

For the following reasons, Applicants respectfully submit that the claims are allowable and request that the application be passed to issue.

No new matter has been added.

II. Claim Objections

Claim 13 was objected, Applicants respectfully submit that the amendment to claim 13 obviates this rejection and therefore request withdrawal of the objection.

III. Claim Rejections 35 U.S.C. § 102(b)/ § 103(a)

Claims 1, 2 and 3 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by or, in the alternative, under § 103(a) as allegedly being unpatentable over Oda et al., U.S. Patent No. 5,644,387 ("Oda"). Applicants respectfully disagree.

Claim 1 recites,

> A memory matrix device for storing temporally sequential information in a manner that retains the sequence of information without dependence on multiple memory addresses, and is not a serial sequential access memory, a random access memory or a dynamic random access memory, comprising:
> sequentially-connected arrays of fixed memory storage units;
> means for applying the temporally sequential information to the arrays of fixed memory storage units; and
> means for successively latching and disabling each successive fixed memory storage unit in a sequentially-connected array of said units, each array becoming enabled and then unenabled in temporal sequence, thereby directing the next temporal bit of information to the next memory storage unit in said sequentially-connected array, and
> wherein, the input to the sequentially-connected array of fixed memory storage units is disabled upon completion of storage of a temporally sequential event to prevent overwriting.

Anticipation under 35 U.S.C. § 102 requires that "each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed Cir. 1987). At a minimum, the cited prior art does not teach or suggest (expressly or inherently) a memory matrix device, comprising,

> sequentially-connected arrays of fixed memory storage units; means for applying the temporally sequential information to the arrays of fixed memory storage units; and means for successively latching and disabling each successive fixed memory storage unit in a sequentially-connected array of said units, each array becoming enabled and then unenabled in temporal sequence.

This configuration is illustrated, for example, in FIG. 8, which shows a matrix in which multiple parallel and perpendicular connected lines serve to input the data, and to distribute it across the arrays, which may be extended in either direction.

In contrast, Oda discloses a device in which the speed at which data can be processed is increased by splitting data across two parallel lines and decreasing the duty cycle. As such, in Oda, the nature of the input is not composed of several parallel lines, but of a single line.

Furthermore, it is clear that Oda discloses a method for a single input line not multiple arrays. As such, Oda provides a means for storing data on a single input line and of very limited information (only across 8 registers). It is, therefore, only suitable for very restricted types of information storage.

Moreover, Oda does not disclose a matrix connecting parallel and perpendicular arrays, as recited in claim 1. Rather, in Oda, since the data is sent through a coherent laser light and is received through a single input line, the information that can be stored is limited in resolution (in both time and space).

Accordingly, Oda fails to teach or suggest all of the claim elements of claim 1, and therefore is allowable.

Furthermore, claims 2, 3, 5 and 6 depend from and further define the subject matter of allowable claim 1, and therefore are also allowable.

IV. Claim Rejections under 35 U.S.C. § 102(b)

Claims 7, 8, 13, and 15 were rejected under 35 U.S.C. § 102(b) as allegedly being unpatentable over Oda. Applicants respectfully disagree.

Claims 7 recites, in pertinent part,

> A memory matrix device for storing temporally sequential information in a manner that retains the sequence of information without dependence on multiple memory addresses, and is not a serial sequential access memory, a random access memory or a dynamic random access memory, comprising:
> sequentially-connected arrays of fixed memory storage units;

> means for applying the temporally sequential information to the arrays of fixed memory storage units; and . . . using the fixed sequentially-connected arrays as a means for subsequently reading each of the fixed memory storage units in a sequentially-connected array, or in multiple parallel sequentially-connected arrays, in the same temporal sequence in which each fixed memory storage unit was initially latched during storage, allowing retrieval of the temporal sequence of stored information without reliance on processing multiple memory addresses.

Similarly claim 13, recites, in pertinent part,

> A method of storing temporally sequential information in an array of sequentially-connected fixed memory storage units . . . the fixed memory storage units are connected in a permanent order such that whenever information is applied to the input and first fixed memory storage unit of a sequentially-connected array, the fixed memory storage units of said array are written to and latched in an invariant order; and whenever a signal generator activates reading at the first fixed memory storage unit of the array, reading of the entire array of fixed memory storage units occurs in the same invariant order.

As such, claims 7 and 13 each require that temporally sequential information **is stored in an array and then is retrieved and read in the same temporal sequence as it was initially stored or latched**. This retrieval mechanism recalls the full sequence of the stored data in time and space across the matrix.

In contrast, Oda does not provide a method for later retrieving the original data in its original sequence. Instead, Oda discloses an instrument which stores secondary information derived from a calculation (e.g., the time-delay between the first and last data point), and must be reset prior to the initiation of a second reading. As such, Oda clearly does not teach a method for replaying the stored information for reanalysis, or to replay the information on repeated occasions.

Accordingly, it is respectfully submitted that claims 7 and 13 are allowable over Oda.

Furthermore, claims 8-11 and 15-19 depend from and further define the subject matter of claims 7 and 13 respectively, and therefore are also allowable.

V. Claim Rejections under 35 U.S.C. § 102(e) or in the alternative § 103(a)

Claim 12 was rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Chai et al., U.S. Patent No. 6,046,947 ("Chai"), or in the alternative under § 103(a), as allegedly being unpatentable over Chai. Applicants respectfully disagree.

Claim 12 recites,

> A memory matrix device for retrieving temporally sequential information, without processing multiple memory addresses, comprising: means for activating a pulse generator or other signal generator to read previously-stored information in sequentially-connected arrays of fixed memory storage units in the sequential order in which said fixed memory storage units are connected;
> means for generating signals transmitted through vertical arrays connecting multiple parallel sequentially-connected arrays (horizontal arrays), to allow simultaneous signal application to temporally corresponding fixed memory storage units and consequent reading of information originating at the same point in time in different parallel horizontal arrays; and
> means for successively reading the fixed memory storage units in the same sequence order in which they were latched during storage, to allow retrieval and temporal recreation of the corresponding stored temporally sequential information.

At a minimum, Chai fails to teach or suggest a device, as recited in claim 12 having "means for successively reading the fixed memory storage units **in the same sequence order in which they were latched during storage, to allow retrieval and temporal recreation of the corresponding stored temporally sequential information**."

Chai discloses a device in which data is outputs a string of data in a pipeline fashion, **not in the same sequence order in which they were latched during storage, nor** allowing for any **temporal recreation of the corresponding stored temporally sequential information** as

recited in claim 12. As such, the data in Chai essentially loses any relationship with time. In fact, it is clear from Chai, that data is simultaneously delivered into a series of registers, and that an artificial sequence for inputting and outputting is used.

Moreover, in Chai, the order of information is irrelevant, and therefore does not teach or suggest a method for storing an original sequence of information. The data in Chai is not stored or read in the same order in the data was latched because the data is input into the eight pipelined registers simultaneously via parallel lines from a memory device and therefore has no sequence based on time.

Furthermore, the device disclosed in Chai converts simultaneous information into a serial output format because the data are given an artificial serial sequence.

The instant subject matter as recited in claim 12, is inherently different in that the instant subject matter requires inputting and storing initially sequential information and at a latter point, reading this information while maintaining the original sequence of the information.

In addition, the device of Chai does not teach or suggest arrays that are enabled sequentially, as recited in claim 12. Instead, Chai discloses serial connections, which are used to output a string of data without maintaining any original temporal sequence. Therefore, the serial output is not a reflection of the original temporal information.

In other words, Chai does not teach or suggest the storage of information in a temporally sequential manner, and therefore cannot read the fixed memory in the same temporally sequential manner. Moreover, in Chai, the storage of information in the pipeline registers is over parallel lines, not sequentially. Finally, and sequence of information being read from the pipeline in Chai is not related to the original sequence of stored information, as recited in claim 12.

Accordingly claim 12 is allowable over the cited prior art references.

VI. Claim 4

Applicants acknowledge, with appreciation, the Examiner objection to Claim 4 as being dependent on a rejected base claim but being allowable if re-written in independent form. As such, claim 4 has been re-written in independent form, including all of the elements of independent claim 1 and intervening claim 3.

Therefore, Applicants respectfully submit that claim 4 is allowable.

VII. Conclusion

In view of the above amendments and remarks, Applicants respectfully submit that this application should be allowed and the case passed to issue. If there are any questions regarding this Amendment or the application in general, a telephone call to the undersigned would be appreciated to expedite the prosecution of the application.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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